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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,138	11/13/2003	Scott B. Kesler	DP-309051	9605

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,138	KESLER, SCOTT B.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-21-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1 the recitation "bias current control circuitry for controlling bias currents **associated** with the first and second transistors, wherein the bias current control circuitry minimizes the bias currents ... and wherein the bias current control circuitry increases the bias currents **associated** with the comparator circuit" is indefinite because it is misdescriptive. Figure 3 of the present application shows that the " bias currents **associated** with the first and second transistors (Q1, Q2) is bias current source (I1). The bias current (I1) is fixed because (I1) is a constant current source. It is not clear what " bias current **associated** with the first and second transistors" is meant by. As understood by the examiner, the recited "bias current" is the current flowing through transistor (Q1) or (Q4). This is merely the collector-emitter current, not the bias current. The Applicant is requested to clarify what are the "bias currents associated with the first and second transistors". The same rationale is applied to the recitation "minimizing bias current" and "increasing the bias current" in claims 10 and 17, "the bias currents are increased" in claim 13. The recitation " when a magnitude ...the reference input terminal" on lines 14-16 is indefinite because it is not clear what the "a predetermined value **from** a magnitude of a reference signal" is meant by. The recitation " the magnitude.... input terminal" on lines 18-20 is indefinite because it is not clear what " **within** the predetermined value of the magnitude of the reference signal" is. A value can be smaller, greater or equal to another value but it cannot be **within** that value. The Applicant is requested to clarify what are the values of the input signal (from, within) with respect to the reference signal. The same rationale is applied to claims 3, 10, 13, 17.

Regarding claims 8 and 19, the recitation "a blinding timer discharge current source..."is indefinite because it is not clear what it is and how it is connected to capacitor (C1) in figures 3 or 6. The Applicant is requested to point out in the drawing the "blinding timer".

Regarding claim 20, the recitation "a switch coupled across the capacitor, wherein the switch is configured to reduce an associated current to substantially **its** leakage current when the switch is off" is indefinite because it is not clear. Figure 6 of the present application shows that switch (Q24) coupled to capacitor (C1) itself cannot reduce its own leakage current.

Claims 2-7, 9, 11, 12, 14-16 and 18 are indefinite because of the technical deficiencies of claims 1, 10 and 17.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7, 10-15, 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Hauge et al. (US Pat. 4,536,717).

Regarding claim 1, 2, 3 and 7, figure 1 of Hauge shows a comparator circuit with controlled outer transistor stage bias currents, comprising:

an outer transistor stage including:

a first transistor (14) including a signal input terminal, a first output terminal and a second output terminal; and

a second transistor (20) including a reference input terminal (col. 3 lines 7-20), a first output terminal and a second output terminal, wherein the first and second output terminals of the first and second transistors are coupled across a power source, and wherein the first and second transistors of the outer transistor stage provide drive currents to transistors of an inner transistor stage; and

bias current control circuitry (16, 22) for controlling bias currents associated with the first and second transistors, wherein the bias current control circuitry minimizes the bias currents when a magnitude of an input signal at the signal input terminal is "a predetermined value from a magnitude of a reference signal" applied to the reference input terminal, and wherein the bias current control circuitry increases the bias currents associated with the comparator circuit when the magnitude of the input signal at the signal input terminal is "within the predetermined value" of the magnitude of the reference signal at the reference input terminal. Note that when the input signal (Vin) is **smaller** than the reference voltage applied to the base of transistor (20), the current flowing through transistor (14) is smaller than the current flowing through transistor (20), thus the current flowing through transistors (14) and (20) is reduced. When voltage (Vin) increases close to the reference voltage, transistor (14) is more biased and the current flowing through transistor (14) increases thus, the "bias currents associated the first and second transistors" increase. Figure 1 comprises bipolar transistors.

Regarding claims 4 and 5, the bias currents have a desired magnitude when the inputs of the comparator are applied with two substantially equal signals. Vin is a non-inverting input.

Regarding claims 10-13, figure 1 of Hauge shows a method for reducing input currents associated with a comparator circuit during certain events, comprising the steps of:

minimizing bias currents associated with a comparator circuit when a magnitude of an input signal (Vi) at a signal input of the comparator circuit is "a predetermined value from a magnitude" of a reference signal applied to a reference input of the comparator circuit (the gate of transistor 20), and

increasing the "bias currents associated with the comparator circuit" when the magnitude of the input signal at the signal input of the comparator circuit is "within the predetermined value" of the magnitude of the reference signal at the reference input of the comparator circuit. Note that when the input (Vin) **increases** close to the reference voltage, the "bias currents associated with the comparator circuit" increase because transistor (14) is turned on harder. Transistors (14) and (20) are in the outer stage. The reference signal is a voltage signal (col. 3, lines 10-20).

Regarding claims 14 and 15, the bias currents have a desired magnitude when the inputs of the comparator are applied with two substantially equal signals. Vin is a non-inverting input.

Regarding claims 17 and 18, figure 1 of Hauge shows an automotive ignition system including a comparator circuit with controlled outer transistor stage bias currents, the comparator circuit comprising:

an outer transistor stage (14, 20);

an inner transistor stage (18, 24);

bias current control circuitry (16, 22) for controlling bias currents associated with the first and second transistors, wherein the bias current control circuitry minimizes the bias currents when a magnitude of an input signal at the signal input terminal is "a predetermined value from a magnitude of a reference signal" applied to the reference input terminal, and wherein the bias current control circuitry increases the bias currents associated with the comparator circuit when the magnitude of the input signal at the signal input terminal is "within the predetermined value" of the magnitude of the reference signal at the reference input terminal. Note that when the input signal is **smaller** than the reference voltage applied to the base of transistor (20), the current flowing through transistor (14) is smaller than the current flowing through transistor (20), thus the current flowing through transistors (14) and (20) is reduced. When voltage Vin increases and close to the reference voltage, transistor (14) is more biased and the current flowing through transistor (14) increases thus the "bias currents associated the first and second transistors" increase. Figure 1 comprises bipolar transistors. Vin is a non-inverting input.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in

the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hauge et al. (US Pat. 4,536,717).

Regarding claims 6 and 16, figure 1 of Hauge includes all the limitations of claims 6 and 16 except for the limitation that the predetermined value is about 50mV. However, it is old and well known and it would have been an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative predetermined value of a differential input voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative predetermined value of a differential input voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III). Therefore, it would have been obvious to one having ordinary skill in the art to select the predetermined value to be 50mV_ dependent upon particular environment of use to ensure optimum performance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
10-20-04

TUAN T. LAM
PRIMARY EXAMINER